|  |  |  |
| --- | --- | --- |
| G:\nsu-logo.png  **North South University**  Department of Electrical & Computer Engineering    **LAB REPORT**  Course Name: **CSE231L**  Experiment Number: 08     |  | | --- | | Experiment Name: **Synchronous Sequential Circuits** |     Experiment Date: 03/01/2021  Report Submission Date: 09/01/2021  Section: | |
| Student Name: Koushik Banerjee | Score |
| Student ID: **1812171642** |  |
| Remarks: |

**LAB-08: Synchronous Sequential Circuits**

**Objectives:**

**Apparatus:**

**Theory:**

**Synchronous Sequential Circuits:**

**State Table:**

**State Diagram:**

**Circuit Diagram:**

**Experiment-1: Figure F1: Constructing a Sequential Circuit using JK Flip-Flop.**

**Experiment-2: Figure F2: Constructing a Sequential Circuit using T Flip-Flop.**

**Experiment-3: Figure F3: Constructing a Sequential Circuit using D Flip-Flop.**

**Data Table:**

**Experiment-1: Table 01: State table for circuit using JK Flip-Flop.**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Present state** | | **Input** | **Next state** | | **Output** | **Flip-flop input functions** | | | |
| **A** | **B** | **X** | **A** | **B** | **Y** | **JA** | **KA** | **JB** | **KB** |
| **0** | **0** | **0** |  |  |  |  |  |  |  |
| **0** | **0** | **1** |  |  |  |  |  |  |  |
| **0** | **1** | **0** |  |  |  |  |  |  |  |
| **0** | **1** | **1** |  |  |  |  |  |  |  |
| **1** | **0** | **0** |  |  |  |  |  |  |  |
| **1** | **0** | **1** |  |  |  |  |  |  |  |
| **1** | **1** | **0** |  |  |  |  |  |  |  |
| **1** | **1** | **1** |  |  |  |  |  |  |  |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |

**JA = KA = JB =**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |

**KB = Y =**

**Experiment-2: Table 02: State table for circuit using T Flip-Flop.**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Present state** | | **Input** | **Next state** | | **Output** | **Flip-flop input functions** | |
| **A** | **B** | **X** | **A** | **B** | **Y** | **TA** | **TB** |
| **0** | **0** | **0** |  |  |  |  |  |
| **0** | **0** | **1** |  |  |  |  |  |
| **0** | **1** | **0** |  |  |  |  |  |
| **0** | **1** | **1** |  |  |  |  |  |
| **1** | **0** | **0** |  |  |  |  |  |
| **1** | **0** | **1** |  |  |  |  |  |
| **1** | **1** | **0** |  |  |  |  |  |
| **1** | **1** | **1** |  |  |  |  |  |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |

**TA = TB** = Y =

**Experiment-3: Table 03: State table for circuit using D Flip-Flop.**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Present state** | | **Input** | **Next state** | | **Output** | **Flip-flop input functions** | |
| **A** | **B** | **X** | **A** | **B** | **Y** | **DA** | **DB** |
| **0** | **0** | **0** |  |  |  |  |  |
| **0** | **0** | **1** |  |  |  |  |  |
| **0** | **1** | **0** |  |  |  |  |  |
| **0** | **1** | **1** |  |  |  |  |  |
| **1** | **0** | **0** |  |  |  |  |  |
| **1** | **0** | **1** |  |  |  |  |  |
| **1** | **1** | **0** |  |  |  |  |  |
| **1** | **1** | **1** |  |  |  |  |  |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |

**DA = DB = Y =**

**Question and Answer:**

**Experiment-2:**

**Ques-01**: Reason behind the output y equation of JK and T be the same

**ANS**:

**Experiment-3: IC Diagram for the logic circuit in T Flip-Flop**

**Discussion:**